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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/629,671	07/30/2003	Hee Bok Kang	40296-0005	6501

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EXAMINER	
NGUYEN, VAN THU T	

ART UNIT	PAPER NUMBER
2824	

DATE MAILED: 12/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,671	KANG, HEE BOK	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *5-9,13,15,16 and 18* is/are pending in the application.

4a) Of the above claim(s) *1-4,10-12,14 and 19* is/are withdrawn from consideration.

5)☒ Claim(s) *15,16 and 18* is/are allowed.

6)☒ Claim(s) *5-9 and 13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/30/03
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Group IV, claims 5-9,13, 15, 16 and 18 in the reply filed on September 28, 2004 is acknowledged.

2. Applicant is requested to cancel claims 1-4, 10-12, 14, and 19 in the next response (Noted that claim 17 is missing from the original set of claims).

Claim Objections

3. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claim 18 should be renumbered as 17.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 5-9, 13 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 5, it is not clear if "a lower byte region of a data I/O buffer", on line 4, is same as that on lines 2-3.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang (U.S. Patent No. 5,373,467) in view of Boler et al. (U.S. Patent No. 5,134,584).

Regarding claim 5, Wang discloses, in FIG. 3, a memory device comprising:

a switch array (32, 34,42) comprising an inherent plurality of first switches (42) for connecting a lower byte region of data lines (16a2 or 16b2) to a lower byte region of a memory array (via 24b), an inherent plurality of second switches (34) for connecting the lower byte region of the data lines (via 16a2 or 16b2) to an upper byte region of the memory array (via 24a), and a plurality of inherent third switches (32) for connecting an upper byte region of a data lines (16a1 or 16b1) to the upper byte region of the memory array (via 24a);

and a switch controller (38, 40, 46, 48) for receiving external control signals (16/8, MSB Add) to control activation of the data lines and on/off operations of the first through the third switches.

(See column 3, line 37 to column 5 line 47).

However, Wang does not disclose that the switches are connected through sense amplifiers and I/O buffers.

Boler et al. disclose, in FIG. 1A, each bit outputted from the memory array via a sense amplifier (24), and output to a data line via a data I/O buffer (26).

Since Wang and Boler et al. are both from the same field of endeavor, the purpose disclosed by Boler et al. would have been recognized in the pertinent art of Wang.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to realize that sense amplifiers and data I/O buffers are essential components in a memory device.

8. Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wang in view of Boler et al. further in view of Kang et al. (U.S. Patent No. 6,775,172)

Wang and Boler et al. disclose, as applied in prior rejection of claim 5, all claimed subject matter except further limitation as in claim 13.

Regarding claim 13, Kang et al. disclose, in FIG. 7, a ferroelectric memory device having a bitline structure comprising a main bitline and a plurality of sub bitlines.

Since Wang, Boler et al., and Kang et al. are all from the same field of endeavor, the purpose disclosed by Kang et al. would have been recognized in the pertinent art of Wang and Boler et al.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to realize the method disclosed in Wang can be applied to all types of memory, and the ferroelectric memory device disclosed in Kang et al. is not an exceptional of use.

Allowable Subject Matter

9. Claims 6-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. Claims 15-16, 18 are allowed.

11. The following is a statement of reasons for the indication of allowance:

The prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Wang, Parks, Boler et al., and Wada et al., taken individually or in combination, do not teach the claimed invention having the following limitations, in combination with the remaining claimed limitations:

(i) wherein the switch controller turns on the first switch and activates the lower byte region of the data lines connected to an inherent I/O port when a lower signal included in the external control signal is activated, and turns on the third switch and activates the upper byte region of the data I/O buffer connected to an I/O port when an upper byte signal included in the external control signal is activated (as in claims 6 and 9).

(ii) wherein the lower byte region of the data I/O buffer is connected to an I/O port, the upper byte region of the data I/O buffer is not connected to an I/O port, and an external control signal included in the external signals is provided through a terminal pin connected to the upper byte region of the data I/O buffer (as in claim 7).

(iii) receiving an address bit on an input for the upper byte portion of the data buffer; and using the address bit received on the input for the upper byte portion of the data buffer to control the output and input of data from/to the system bus (as in claim 15).

(iv) receiving a data byte and a one-byte address for the data byte from the system, the one-byte address having a least significant bit, wherein the least significant bit is received as an input to a upper byte portion of a data input/output; and storing the received data byte to either the upper byte portion or the lower byte portion associated with the address in response to the least significant bit. (as in claim 16).

(v) a circuit that stores data of the lower byte portion of the data input/output buffer to either an upper byte portion or a lower byte portion of data storing portion depending upon an external signal received on a data pad coupled to the upper byte portion of the data input/output buffer (as in claim 18).

Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Friday, 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VTN
November 27, 2004

VanThu Nguyen
Primary Examiner
Art Unit 2824